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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,327	02/11/2004	Jun Koyama	0756-7255	8544
31780	7590	03/10/2006	EXAMINER	
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			SOWARD, IDA M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/775,327

Applicant(s)

KOYAMA ET AL.

Examiner

Ida M. Soward

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 2-37 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-37 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12-22-2005.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

This Office Action is in response to the Applicants' amendment filed December 22, 2005.

### ***Priority***

This application filed under former 37 CFR 1.60 lacks the necessary reference to the prior application. A statement reading "This is a Divisional of Application No. 09/309,891, filed May 11, 1999." should be entered following the title of the invention or as the first sentence of the specification. Also, the current status of all nonprovisional parent applications referenced should be included.

### ***Specification***

The objection to the abstract has been withdrawn due to the amendment filed.

The objection to the title of the invention has been withdrawn due to the amendment filed.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-9 and 30-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahara (US 6,219,113 B1).

In regard to claim 2, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12; a data line driver circuit 541 over the substrate 12; and a dividing circuit 2165 over the substrate 12 (Figures 56 and 216; columns 62-63 and 126; lines 53-67, 1-23 and 1-14, respectively).

In regard to claim 3, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12; a data line driver circuit 541 comprising a plurality of NAND circuits over the substrate 12; and a dividing circuit 2165 over the substrate 12 (Figures 56 and 216; columns 62-63, 89 and 126; lines 53-67, 1-23, 48-63 and 1-14, respectively).

In regard to claim 4, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12; a data line driver circuit 541 over the substrate 12; a dividing circuit 2165 over the substrate 12 (Figures 56 and 216; columns 62-63 and 126; lines 53-67, 1-23 and 1-14, respectively).

In regard to claim 5, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12; a data line driver circuit 541 comprising a plurality of NAND circuits over the substrate 12; and a dividing circuit 2165 over the substrate 12 (Figures 56 and 216; columns 62-63, 89 and 126; lines 53-67, 1-23, 48-63 and 1-14, respectively).

In regard to claim 6, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12, each of the plurality of pixels having a thin film transistor 155; a data line driver circuit 541 over the substrate 12; and a dividing circuit 2165 over the substrate 12 (Figures 35, 56 and 216; columns 46, 62-63 and 126; lines 49-67, 53-67, 1-23 and 1-14, respectively).

In regard to claim 7, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12, each of the plurality of pixels 14 having a thin film transistor 155; a data line driver circuit 541 comprising a plurality of NAND circuits over the substrate 12; and a dividing circuit 2165 over the substrate 12 (Figures 35, 56 and 216; columns 46, 62-63, 89 and 126; lines 49-67, 53-67, 1-23, 48-63 and 1-14, respectively).

In regard to claim 8, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12, each of the plurality of pixels 14 having a thin film transistor 155; a data line driver circuit 541 over the substrate 12; a dividing circuit 2165 over the substrate 12 (Figures 35, 56 and 216; columns 46, 62-63 and 126; lines 49-67, 53-67, 1-23 and 1-14, respectively).

In regard to claim 9, Takahara et al. teach a semiconductor device comprising: a plurality of pixels 14 over a substrate 12, each of the plurality of pixels 14 having a thin film transistor 155; a data line driver circuit 541 comprising a plurality of NAND circuits over the substrate 12; and a dividing circuit 2165 over the substrate 12 (Figures 35, 56 and 216; columns 46, 62-63, 89 and 126; lines 49-67, 53-67, 1-23, 48-63 and 1-14, respectively).

In regard to claims 30-37, Takahara et al. teach the semiconductor device applied to a google type display (Figures 152-154).

However, Takahara et al. fail to explicitly teach the various functions of the dividing circuit.

In regard to the dividing circuit dividing a signal into  $n$  signals, wherein the  $n$  signals inputted into corresponding  $n$  pixels by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing a signal into  $n$  signals, wherein the  $n$  signals inputted into corresponding  $n$  pixels by a timing signal supplied from one of the plurality of NAND circuits, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into  $3n$  signals, wherein the  $3n$  signals are inputted into corresponding  $3n$  pixels by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than

function, *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into  $3n$  signals, and wherein the  $3n$  signals are inputted into corresponding  $3n$  pixels by a timing signal supplied from one of the plurality of NAND circuits, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing a signal into  $n$  signals, and wherein the  $n$  signals are inputted into thin film transistors corresponding  $n$  pixels by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing a signal into  $n$  signals, and wherein the  $n$  signals are inputted into thin film transistors corresponding to  $n$  by a timing signal supplied from one of the plurality of NAND circuits, pixels simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure

rather than function, *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into 3n signals, wherein the 3n signals are inputted into thin film transistors corresponding to 3n pixels by a timing signal supplied from the data driver circuit, simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to the dividing circuit dividing three signals corresponding to colors R, G and B into 3n signals, and wherein the 3n signals are inputted into thin film transistors corresponding to 3n by a timing signal supplied from one of the plurality of NAND circuits, pixels simultaneously, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, *In re Danly*, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was for the semiconductor device structure as taught by



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Takahara et al. to perform the various functions of the dividing circuit to provide a liquid crystal display device that consumes less power.

Claims 10-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahara et al. (US 6,219,113 B1) as applied to claims 2-9 and 30-37 above, and further in view of Yamazaki (6,115,097).

Takahara et al. teach all mentioned in the rejection above.

However, Takahara et al. fail to teach the data line driver circuit comprising a shift register, NAND circuits, a level shifter and a buffer; the substrate comprising glass; and the thin film transistor comprising polycrystalline silicon film.

Yamazaki teaches a data line driver circuit comprising a shift register, NAND circuits, a level shifter and a buffer (column 10, lines 33-36); a substrate 401 comprising glass (Figure 4A, column 3, lines 51-54); and a thin film transistor comprising polycrystalline silicon film (column 1, lines 26-29).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was modify the semiconductor device structure as taught by Takahara et al. with the semiconductor device having a data line driver circuit comprising a shift register, NAND circuits, a level shifter and a buffer; and a substrate comprising glass as taught by Yamazaki to provide a semiconductor device capable of being used as a display of portable video cameras and portable business equipment, and further of various types of information terminal equipment (column 1, lines 44-52).

***Response to Arguments***

Applicant's arguments concerning the art rejections with respect to claims 2-37 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments concerning the functional language filed 12-22-2005 have been fully considered but they are not persuasive. The claimed invention is drawn to a semiconductor device structure. What is patentable is the structure of the semiconductor device not what the structure does.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to pixel structures:

Furuhashi et al. (6,127,995)

Kikuo et al. (5,250,937)

Sato et al. (5,712,652).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS

March 3, 2006

*J. M. Samard*  
*AU 2822*